What is claimed is:

1. An apparatus for generating a radio frequency (RF) signal and control signals in which the current output from each of a plurality of light receiving elements is converted into voltage signals and the RF signal and the control signals are generated in response to the voltage signals, the apparatus comprising:

an input data processing unit for performing time-sharing sampling on the voltage signals and converting the voltage signals into first digital signals in response to an analog/digital conversion clock signal having a predetermined period and a sequentially applied selection signal;

a digital filter for filtering each of the first digital signals to modify the shape of the waveforms of the first digital signals and outputting the modified waveforms as second digital signals;

a servo signal generating unit for correcting delay time of the second digital signals and generating the control signal for servo control in response to the corrected second digital signals;

a digital RF data generating unit for correcting delay time of the second digital signals before summing the corrected second digital signals to generate digital RF data; and

a reference comparator for comparing an average value of the digital RF data with the voltage level of the digital RF data in response to a predetermined demodulation clock signal and generating a non-return to zero (NRZ) signal in response to a compared result.

2. The apparatus as claimed in claim 1, further comprising:

a phase locked loop (PLL) for generating the analog/digital conversion clock signal having n-times the frequency of the frequency of a channel bit clock signal in response to the digital RF data; and

a timing generating unit for dividing the frequency of the analog/digital conversion clock signal n times to generate the demodulation clock signal and counting the analog/digital conversion clock signal to generate a selection signal of the multiplexer.

3. The apparatus as claimed in claim 2, wherein the timing generating unit includes a counter which is implemented by a modulo-N counter for generating the selection signal in response to a value to which the analog/digital conversion clock signal is counted, and a frequency divider for dividing the frequency of the analog/digital conversion clock signal n times to generate the demodulation clock signal.

4. The apparatus as claimed in claim 3, wherein the counter is implemented by a modulo-4 counter.

5. The apparatus as claimed in claim 3, wherein the frequency divider divides the frequency of the analog/digital conversion clock signal four times.

6. The apparatus as claimed in claim 2, wherein the input data processing unit includes a multiplexer for sequentially outputting the voltage signals in response to the selection signal, and an analog/digital converter (ADC) for performing time-sharing sampling output of the multiplexer in response to the analog/digital conversion clock signal and outputting the sampled signals as the digital signals.

7. The apparatus as claimed in claim 2, wherein the digital filter includes a plurality of finite impulse response (FIR) filters.

8. The apparatus as claimed in claim 2, wherein the servo signal generating unit includes:

a first delaying unit for: (i) delaying a first signal of first through fourth signals, each having a different delay time, by a time 1T, where 1T is a channel bit clock period, in a case where the second digital signals are the first through fourth signals, and (ii) outputting a delayed first signal;

a second delaying unit for delaying a second signal of the first through fourth signals by the time1T and outputting a delayed second signal;

a first adder for adding the delayed first signal to a third signal and outputting the added result as a first adder output signal;

a second adder for adding the delayed second signal to a fourth signal and outputting the added result as a second adder output signal;

a phase discriminator for determining a phase difference between the first adder output signal and the second adder output signal and generating a tracking error in response to the determined result; and

a subtracter for subtracting the second adder output signal from the first adder output signal and outputting the subtracted result as a focusing error.

9. The apparatus as claimed in claim 8, wherein the digital RF data generating unit includes:

a third delaying unit for delaying the first signal by the time 1T and outputting the delayed first signal;

a fourth delaying unit for delaying the second signal by the time1T and outputting the delayed second signal; and

a third adder for adding signals output from the third and fourth delaying units to the third signal and the fourth signal and outputting the added result as the digital RF data.

10. The apparatus as claimed in claim 9, wherein the reference comparator includes:

an average value generating unit for receiving the digital RF data in response to the demodulation clock signal and obtaining the average value of the digital RF data to set the average value of a reference voltage;

a comparator for comparing the reference voltage with the digital RF data and outputting the compared result; and

a data decision unit for deciding whether the period of an output signal of the comparator is a signal existing within a predetermined range and outputting the output signal of the comparator as the NRZ signal in response to the decided result.

11. A method for generating a radio frequency (RF) signal and control signals in which the current output from a plurality of light receiving elements is converted into voltage signals and the RF signal and the control signals are generated in response to the voltage signals, the method comprising the steps of:

(a) performing time-sharing sampling on the voltage signals and generating first digital signals in response to an analog/digital conversion clock signal having a predetermined period and a sequentially applied selection signal;

(b) filtering each of the first digital signals to modify the shape of waveforms of the first digital signals and outputting the modified waveforms as second digital signals;

(c) correcting delay time of the second digital signals and generating the control signals including a focusing error and a tracking error in response to the corrected second digital signals; and

(d) correcting delay time of the second digital signals and generating the RF signal in response to the corrected second digital signals.

12. The method as claimed in claim 11, wherein step (a) includes:

(a1) sequentially outputting the voltage signals in response to the selection signal; and

(a2) sampling the voltage signals sequentially output in response to the analog/digital conversion clock signal, converting the sampled voltage signal into digital signals, and outputting the digital signals.

13. The method as claimed in claim 12, wherein step (c) includes:

(c1) delaying first and second signals having a different delay time by the time 1T, where 1T is a channel bit clock period, and outputting delayed first and second signals, respectively; and

(c2) subtracting the sum of the delayed second signal and a fourth signal from the sum of the delayed first signal and a third signal and generating the focusing error, in the case where the second signals are the first through fourth signals;

determining a phase difference between the sum of the delayed first signal and the third signal and the sum of the delayed second signal and the fourth signal and generating the tracking error in response to the determined result.

14. The method as claimed in claim 13, wherein step (d) includes:

(d1) delaying the first and second signals among the second digital signals having a different delay time, by the time 1T;

(d2) adding the delayed first and second signals to the third and fourth signals and outputting digital RF data;

(d3) comparing an average value of the digital RF data with the digital RF data to generate a non-return to zero (NRZ) signal and outputting the NRZ signal as the digital RF signal.

15. The method as claimed in claim 14, further comprising:

(e) generating a channel bit clock signal synchronized with the digital RF data;

(f) generating a signal having n times the frequency of the channel bit clock signal as the analog/digital conversion clock signal; and

(g) counting the analog/digital conversion clock signal and generating the selection signal in response to the counted result.